Internal BJT Low Standby-Power Primary-side Converter

General description

The PN8571P consists of a Low Standby-Power Primary-Side controller and BJT, specifically designed for a high performance AC/DC charger or adaptor with minimal external components.

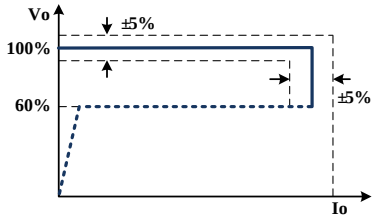
PN8571P operates in primary-side sensing and regulation, so opto-coupler and TL431 could be eliminated. In CV mode, multi-mode technique is utilized to achieve high efficiency, avoid audible noise and make the system meeting Energy star level VI. Good load regulation is achieved by the built-in cable drop compensation. In CC mode, the current and output power setting can be adjusted externally by the sense resistor at CS pin.

PN8571P offers complete protections including Cycle-by-Cycle current limiting protection (OCP), over voltage protection (OVP), open loop protection (OLP), over temperature protection (OTP) and CS open or short protection (CS O/SP) etc.

Application

- Switch AC/DC Adapter
- Battery Charger
- Set-top box power supply

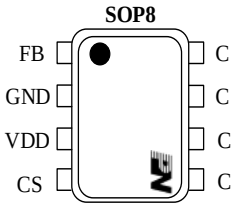
Output Features



Features

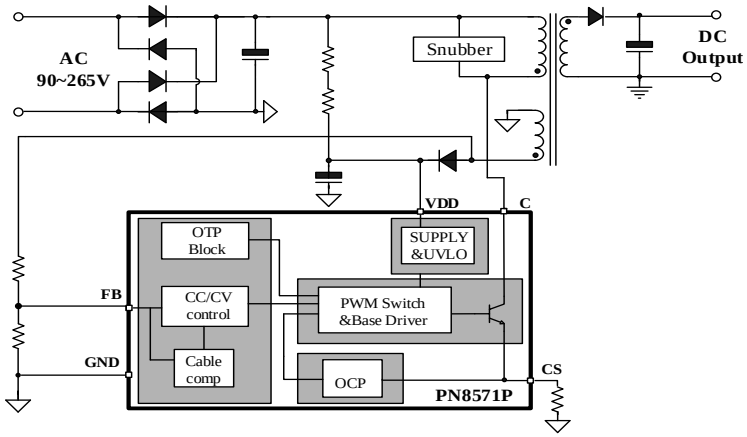
- Internal BJT switch
- Multi-mode technique
- ±5% CC Regulation at Universal AC input
- Primary-side Sensing and Regulation without TL431 and Opto-coupler
- Programmable Cable Drop Compensation
- No-need Control Loop Compensation Capacitor
- Excellent Protection include:
  - ✧ Over Temperature Protection (OTP)
  - ✧ VDD Under/Over Voltage Protection(UVLO&OVP)
  - ✧ Cycle-by-Cycle Current Limiting (OCP)
  - ✧ CS Short/Open Protection (CS O/SP)
  - ✧ Open Loop Protection(OLP)

Package/Order Information



Order code	Package	Typical Power $90\sim265V_{AC}$
PN8571PSEC-R1	SOP8	12W

Typical Circuit



Pin Definitions

Pin Name	Pin Number	Pin Function Description
FB	1	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
GND	2	Ground
VDD	3	Power supply
CS	4	Current Sense Input
C	5,6,7,8	HV BJT collector pin

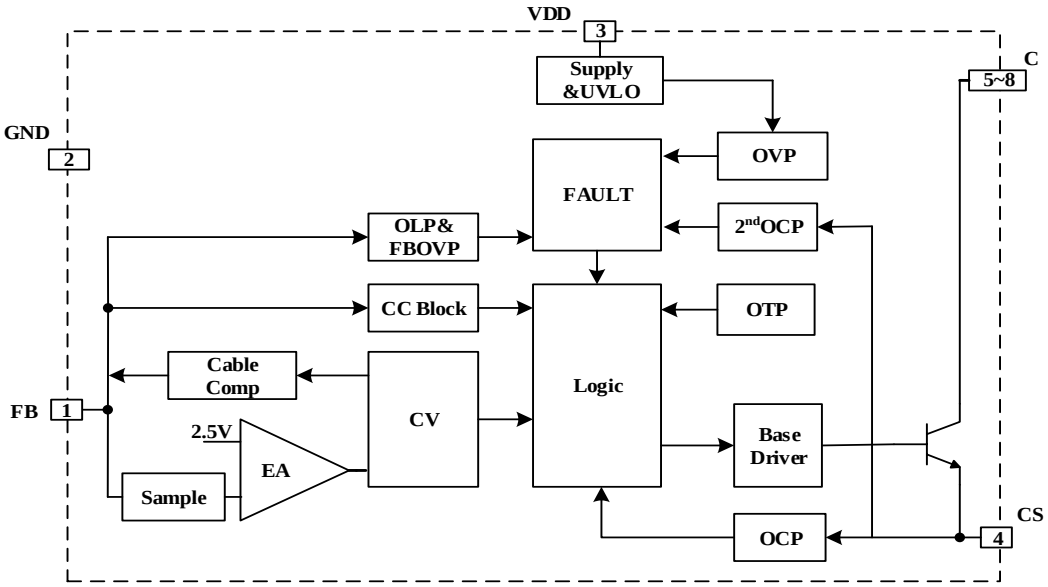
Typical Power

Part number	Package	Adapter(1)
		90~265V_{AC}
PN8571P	SOP8	12W

Note:

1. Maximum output power is tested in an adapter at 40℃ ambient temperature, with enough cooling conditions.

Block Diagram



Absolute Maximum Ratings

Supply voltage Pin VDD…….....……-0.3~40V
Pin FB(I_{FB}≤10mA) ……...……..……-1~5.5V
Pin CS ……...……-0.3~5.5V
CB voltage ……..……700V
Operating Junction Temperature…….....……-40~150 ℃

Storage Temperature Range……...…. ….-55~150 ℃
Lead Temperature (Soldering, 10Secs)……...260 ℃
Package Thermal Resistance θ_{JC} （SOP8）...…40 ℃ /W
HBM ESD Protection (1) ……...…..……..…..±3kV

Note：
1. Test standard: ANSI/ESDA/JEDEC JS-001-2017.

Electrical Characteristics

(T_A= 25 ℃, VDD=21V, unless otherwise specified)

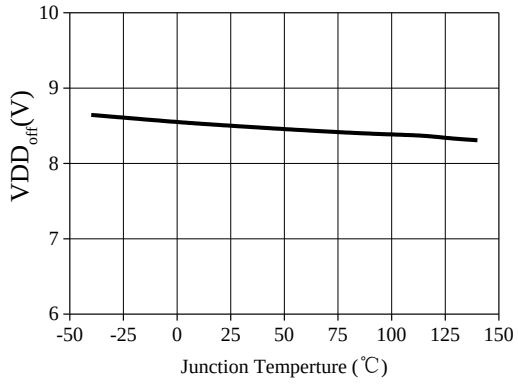
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Section						
Collector-base breakdown voltage	V_{CBO}	I_C=10mA	700			V
Collector-emitter breakdown voltage	V_{CEO}	I_C=10mA，I_B=0	400			V
Collector Peak Current	I_C				0.75	A
Supply Voltage Section						
Operating voltage range	VDD		9.5		30	V
VDD start up threshold	VDD_{on}		14.5	16.5	18.5	V
VDD under voltage shutdown threshold	VDD_{off}		7.5	8.5	9.5	V
VDD over voltage protect	VDD_{ovp}		30	32	35	V
Supply Current Section						
VDD charge current	$I_{DD\_STARTUP}$	VDD=VDD_{on} – 0.5V		3	5	uA
Operating current, switching	I_{DD}	VDD = VDD_{on} +1V	0.1	0.6	0.8	mA
Operating current after fault	I_{DD_FAULT}	VDD＝15V after fault		0.5		mA
Current Sense Section						
Current sense threshold	V_{TH_OC}(1)		485	500	515	mV
Maximum Current sense threshold	$V_{TH\_OC\_MAX}$(1)			560		mV
Minimum CS threshold	Vcs_min			170		mV
Leading Edge Blanking time	T_{LEB}			300		ns
Maximum Ton	T_{onmax}		32	40	50	us
OCP propagation delay	T_{D_OC}			100		ns
FB Section						
Reference voltage for feedback threshold	V_{REF_CV}		2.455	2.48	2.52	V
Output over voltage protection threshold	V_{FBOVP}		2.85	3	3.15	V
Output under voltage threshold	V_{UVP}			1.55		V
Maximum cable compensation current	Icable	V_{FB}=0V	33	36	39	uA

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Minimum Toff	T_{offmin}			5		us
Maximum Toff	T_{offmax}			2.2		ms
Output under voltage protection Blanking time	T_{UVP}	F_S= 50kHz	40		64	ms
Thermal Section						
Thermal shutdown temperature threshold	T_{SD}		135	150		℃
Thermal shutdown hysteresis	T_{HYST}			30		℃

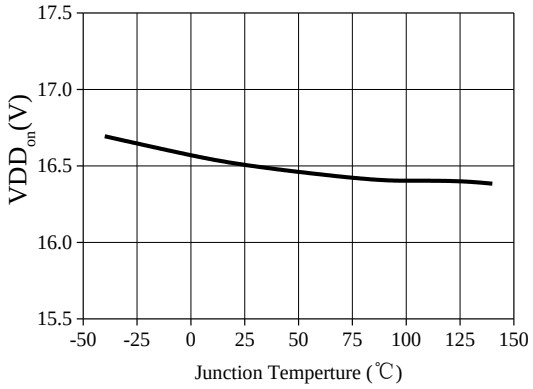
Note:

(1)This parameter is the real measurable value of circuit delay and switch delay, which should be considered in the actual test and design.

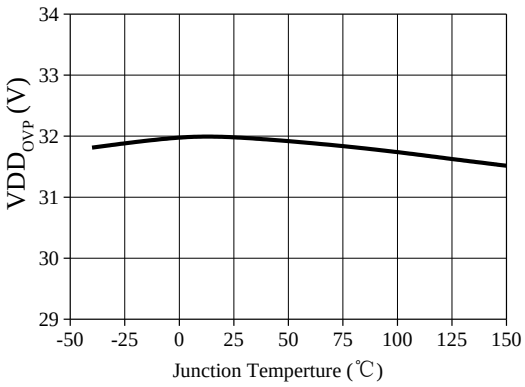
Typical Characteristics Plots



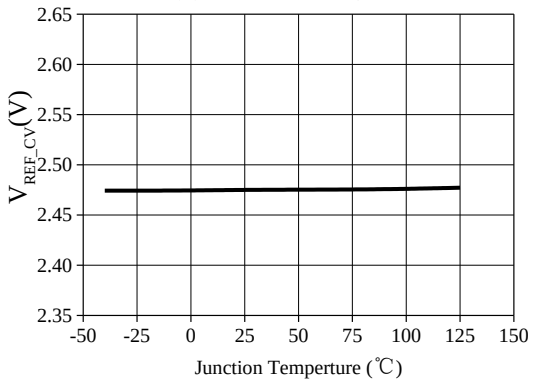
(a) VDD_{off} VS T_j



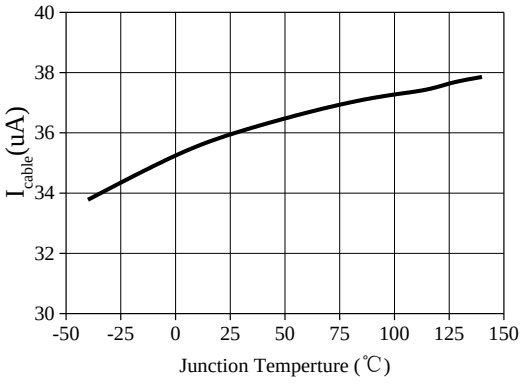
(b) VDD_{on} VS T_j



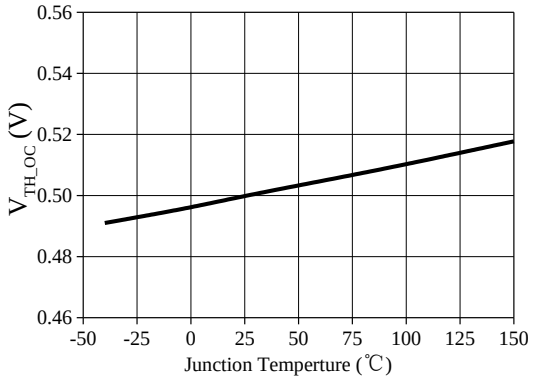
(c) VDD_{OVP} VS T_j



(d) V_{REF_CV} VS T_j



(e) I_{cable} VS T_j



(f) V_{TH_OC} VS Tj

Functional Description

The PN8571P is a high performance CC/CV primary-side controller. PN8571P operates in primary-side sensing and regulation, so opto-coupler and TL431 could be eliminated. Proprietary built-in CV and CC control can achieve high precision CC/CV control meeting most charger and adapter application requirements. Startup current of PN8571P is designed to be very low so a large value startup resistor can be used to minimize the power loss in application.

1. Start up Control

At start up, external startup resistor charges the VDD capacitor via VDD pin. When VDD reaches VDD_{on}, the device starts switching. The device keeps in normal operation provided as long as VDD keeps above VDD_{off}. After startup, the bias is supplied from the auxiliary transformer winding.

2. CC Operation Mode

In CC operation mode, the PN8571P captures the auxiliary flyback signal at FB pin through a resistor dividing-network. The pulse width of the auxiliary flyback signal determines the PN8571P oscillator frequency. The higher the output voltage is, the shorter the pulse width is, and the higher the chip oscillator frequency is, thus the constant output current can be achieved.

The current waveform in DCM mode is shown in Fig.1. During BJT turn-on time, the current in the primary winding (Ipri) ramps up. When BJT turns off, the energy stored in the primary winding is transferred to the secondary side, so the peak current in the secondary winding is

$$I_{sec\_pk} = I_{pri\_pk} \times N_{ps} \qquad (1)$$

The output average current is

$$I_O = \frac{I_{sec\_pk}}{2} \times \frac{T_{demag}}{T_P} = \frac{1}{2} N_{PS} \frac{V_{CS}}{R_{sense}} \frac{T_{demag}}{T_P} \qquad (2)$$

Where Rsense means system resistor at CS pin, N_{PS} means primary winding and secondary winding turn ratio.

In CC mode, PN8571P fixes $\frac{T_{demag}}{T_P}$ to be 0.5, and V_{CS} to be V_{TH_OC} (typically 0.5V, actually about 0.58V considering the affection of system and delay time). Meanwhile, assuming the current coupling ratio is Kc，the output current will be constant as:

$$I_O = \frac{1}{4} N_{PS} \frac{0.58}{R_{sense}} \times Kc \qquad (3)$$

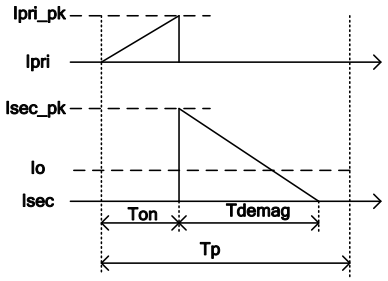


Fig.1 The current waveform in DCM mode

3. CV Operation Mode

In CV mode，PN8571P uses a pulse to sample V_{FB} and it is hold until the next sampling. The sampled voltage is compared with V_{REF_CV} and the error is amplified. The error amplified output reflects the load condition and controls the switching off time to regulate the output voltage, thus constant output voltage can be achieved.

The relationship between the output voltage and V_{REF_CV} is

$$Vo = (V_{REF\_CV} \times \frac{R1+R2}{R2}) \times \frac{N_S}{N_{AUX}} \qquad (3)$$

N_S means Secondary winding truns, N_{AUX} means Auxiliary winding truns.

The PN8571P operates in PFM mode during full load mode, since the peak current (Ipeak) of BJT is constant, the chip frequency decreases while the output current decreases. When the switching frequency approaches to 25kHz, the PN8571P enters PWM mode, the chip frequency decreases slowly while the output current decreases, the Ipeak decreases while the output current decreases. Therefore the PN8571P can avoid audible noise, while achieving high efficiency at 25% load conditions. When Vcs decreases to 170mV, the PN8571P enters Standby mode. In this mode, Ipeak keeps around constant, the chip oscillator frequency decreases while the output current decreases. Fig.2 illustrates the relations of the switching frequency, Ipeak and Loading for PN8571P.

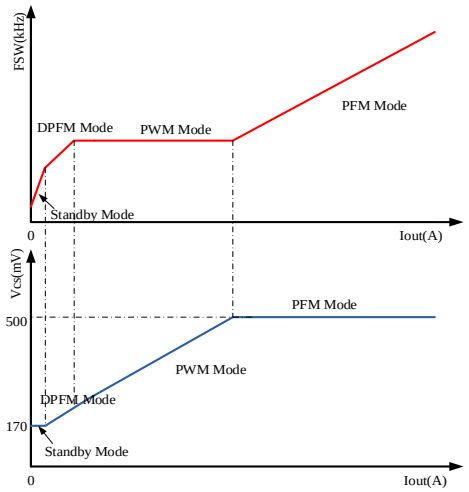


Fig.2 The Switching Frequency, V_{CS} VS. LOAD

4. Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in PN8571P. The switch current is detected by a sense resistor at CS pin. The CC set-point and maximum output power can be externally adjusted by external current sense resistor at CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power BJT on-state so that the external RC filtering on sense input is no longer needed.

5. Programmable Cable Drop Compensation

In PN8571P, an offset voltage is generated at FB pin by an internal current flowing into the divider resister, as shown in Fig.3. The Cable Drop Compensation block compensates the voltage drop across the cable. As the load current decreases from full load to no load, the voltage drop across the cable decreases. It can be programmed by adjusting the external resistor R2 or R1 at FB pin. The maximum compensation is

$$\frac{V_{cable}}{V_O} = \frac{I_{cable} \times (R2 // R1)}{2.5V} \quad (4)$$

Because of the influence of the chip's sampling position and devices of the system, the actual maximum compensation is less than theoretical value.

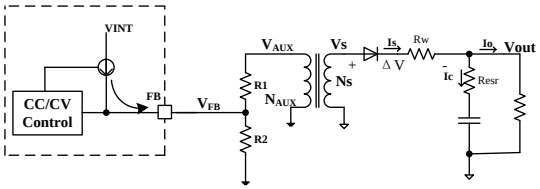
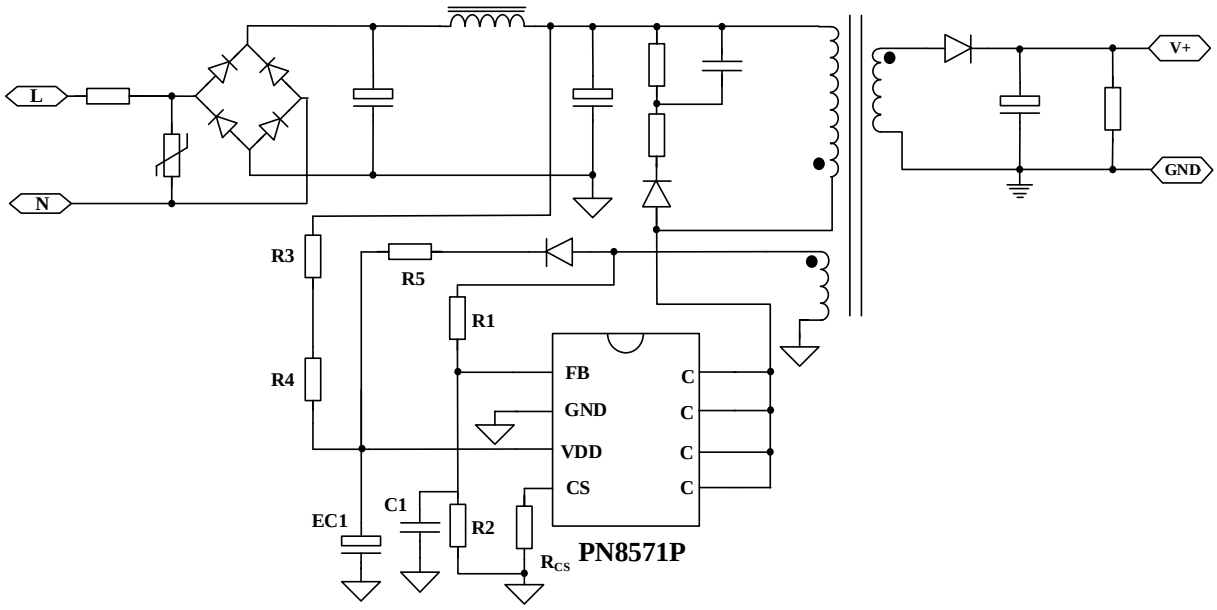


Fig.3 Icable

6. Protection Control

The PN8571P has several self-protection functions, such as Cycle-by-Cycle current limiting (OCP), Over-Voltage Protection, Over-Temperature Protection, Feedback Loop open Protection, Output short circuit Protection, CS resistor open/short circuit Protection and Under Voltage Lockout on VDD. All protections are self-recovered.

Typical Application

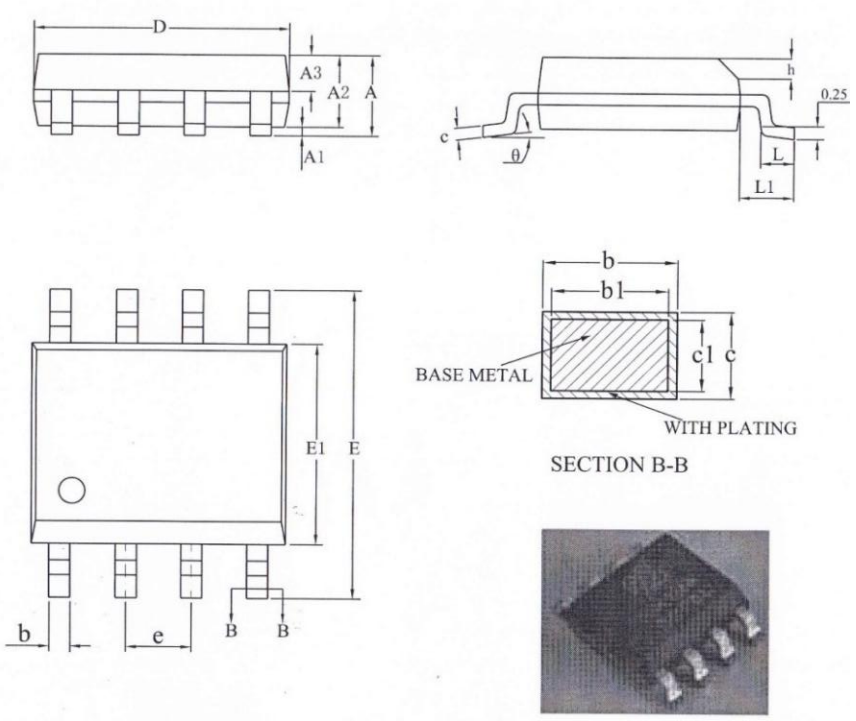


Component Parameter and Layout Considerations:

1. VDD capacitor EC1 should be placed at the nearest place between the VDD pin and the GND pin.
2. It is suggested that the power supply diode and the R5 should be connected in series in order to improve the safety capability. The recommend value is 4.7ohm.
3. It is suggested that the FB pin and the C1 should be connected in parallel in order to improve the anti-interference of the sampling network. The recommend value is 47pF.
4. Choose CS resistance reasonably to avoid IC exceeding 0.75A.

Package Information

Package Information SOP8



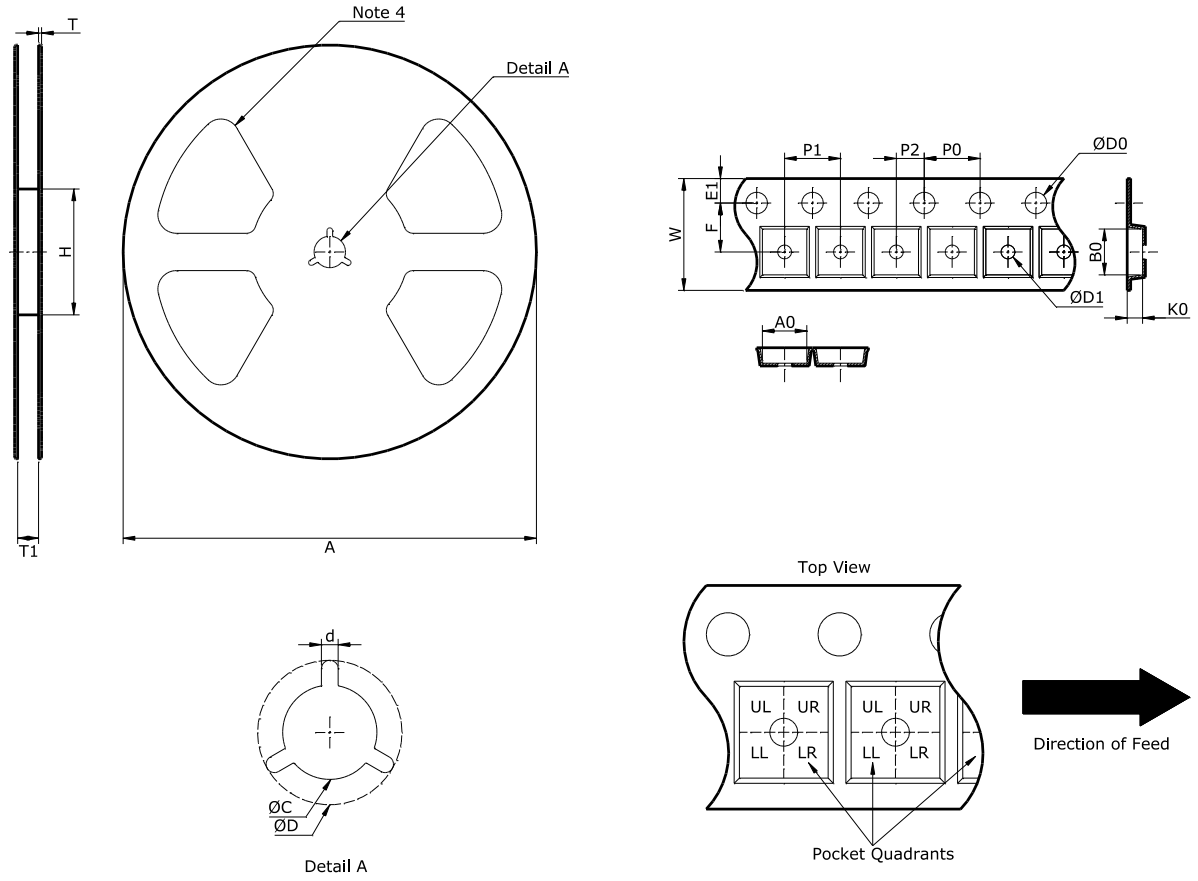
Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)
A	—	—	1.75	D	4.80	4.90	5.00
A1	0.10	—	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.80	3.90	4.00
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	—	0.47	h	0.25	—	0.50
b1	0.38	0.41	0.44	L	0.50	—	0.80
c	0.21	—	0.24	L1	1.05REF		
c1	0.19	0.20	0.21	θ	0	—	8 °

Top mark	Package
PN PN8571P YWWXXXXX	SOP8

Note: Y: Year Code; WW: Week Code; XXXX: Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Tape and Reel Information



SOP8 Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330 ±1.0	3 +1/−0	12.4 +1/−0	100 ±0.5	12.00 +0.5/−0.2	17.70 ±0.40	2.00 +0.5/−0.2	6.60 ±0.1	5.3 ±0.1	1.9 ±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
12.00 ±0.1	5.50 ±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.1	1.5 +0.1/−0	1.55 ±0.05	UL	

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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